REMARKS

In the outstanding Official Action, the drawing was objected to because the component 230 of Fig. 2 is not explained in the specification. In response, and in order to overcome the objection, the instant specification is herewith amended in order to conform the specification to the drawing by clarifying that the external power supply line 130 is coupled by line 230 by a contact 222 of battery container 220. It is respectfully submitted that no new matter is added by this amendment, since Fig. 2 of the drawing clearly shows that the described coupling between the external power supply line and the contact is via line 230, as clearly shown in Fig. 2.

Claim 1 was rejected under 35 USC 112 because the recitation of "by biasing the second gate voltage" was interpreted to suggest the existence of a second gate of the enabled transistor. More particularly, however, the term "second gate voltage" in fact applies to a second voltage applied to the gate, rather than the presence of a second gate, as clearly described and shown in the instant application. Accordingly, claim 1 is herewith amended in order to more precisely recite that the gate is biased with the second gate voltage, to clarify that there is only one gate to which various voltages are applied. It is respectfully submitted that this amendment is in accordance with the interpretation of the

Examiner as presented in the Action, and that claim 1, as herein amended, now fully complies with the requirement of Section 112.

With reference to the rejection of claim 2 under §112 as failing to comply with the enablement requirement, it was suggested in the Action that the claim contains subject matter which was not described in the specification in an enabling manner. In response, it is respectfully submitted that the specification does in fact contain an enabling description of the subject matter in claim 2 relating to the transistor having a substrate and the substrate being coupled to a bias voltage source. Specifically, the instant specification, at page 5, lines 18-20, expressly teaches that the substrate of transistor 154 is coupled to a back biased source 170 via the back biased power supply line 140. Furthermore, this subject matter is schematically illustrated in Fig. 1, by the presence of a dashed line between back biased source 170 and transistor 154. In this regard, it is noted that Fig. 1 of the instant application is a partially schematic and partially block diagram of the instant invention, not a physical or a cross-sectional depiction of a semiconductor device, so that the coupling described in the specification and shown in Fig. 1 are sufficient to enable one skilled in the art to make and/or use the invention.

On the merits, claim 1 was rejected under 35 USC 102(b) as being anticipated by Ye et al, and claim 4 was rejected under 35 USC 103(a) as being unpatenable over Ye (in view of) Hoffman, for

the reasons of record. Although it is indicated in the Summary of the Action that claims 1-4 are rejected, no specific rejection of claims 2 and 3 appears to be made in the Detailed Action.

In response to the section 102 rejection of independent claim 1, claim 1 is herewith amended in order to more particularly and precisely recite that the enabled transistor is biased in the nonconductive state with the second gate voltage, which is obtained from a back biased power supply line (140) which is separate from the external power supply line (130). It is respectfully submitted that this additional limitation in the independent claim is neither shown nor suggested in Ye, which teaches on the contrary, that his corresponding bias voltage for the gate of transistor L1 is obtained through a voltage decreasing circuitry 315 from a power supply line (GND) which is one and the same as the external power supply line (GND) applied to the transistor L1, as shown in the cited figure (Fig. 3) of the reference. Thus, whereas the enabled transistor L1 in the reference has both its gate and main current path coupled to the same external power supply line, the circuit of the invention, as now more clearly and precisely recited, clearly is directed to a substantially different arrangement, in which the gate of the enabled transistor is coupled to a different power supply line than that connected to the main current path of the transistor. It is by this means that a substantial back bias is

applied to the gate of the enabled transistor to dramatically reduce the leakage current in the circuit.

In view of the foregoing amendments and remarks, it is respectfully submitted that the objection to the drawing has been overcome, the rejection of claims 1 and 2 under §112 has been overcome, and independent claim 1, as herein amended, and the remaining claims depending therefrom, have been clearly patentably distinguished over the cited and applied art. Accordingly, allowance of the instant application is respectfully submitted to be justified at the present time, and favorable consideration is earnestly solicited.

Respectfully submitted,

By _____
Steven R. Biren,
Reg. 26,531
(914) 333-9630

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